GODIL
USER MANUAL
V 0.91

OHO-Elektronik
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2. Introduction

GODIL is a low cost and versatile Spartan 3E FPGA module with an optional DIL 0.6” 48 or 40 pin connector to replace legacy DIL devices, or IDC headers only in a 0.1” grid.
Many additional features like USB (future upgrade) make it useful and flexible:

2.1. GODIL Features:

- Low cost
- XC3S500E-4VQG100C FPGA, a member of the XILINX Spartan-3E family
- optional XC3S250E-4VQG100C or XC3S100E-4VQG100C FPGA
- SPI Flash configuration device
- Future USB update
- choice of 0.6” 48 or 40 pin DIL connector with almost arbitrary VCC or GND connection by jumpers
- or 2 x 50 pin IDC 0.1” headers only
- Xilinx Parallel Cable IV or Platform USB (II) Cable compatible download connector 14pin / 2mm, an OHO-Elektronik low cost programmer is also available – GOP_LCP
- 32 (16) Mbit user SPI FLASH
- Operating voltage from 3,5V to 5.5V, switching regulator for core voltage 1,2V
- Voltage translators for 5V I/O compatibility, pullups to 5V
- Voltage translators can be selectively bridged by series resistors
- Onboard clock oscillator with 49.152 MHz for audio or RS232 applications
- up to 9 status or user leds, 2 user tact switches, 2 configuration jumper
- A 9-pin test connector for probing internal signals or using the OHO_DY1 debug display
- Reverse plug in protection
- Easy to reuse
- Professional design, manufactured on a 4 layer PCB, made in Germany

2.2. GODIL Applications:

- Replacement of discontinued 24-48 pin 0.6” DIL devices
- IP core development system for legacy or brand new DIL chips
- OEM Spartan 3E FPGA module with up to 48 I/O’s and 2 input onlies
- Fast evaluation of Xilinx Spartan-3E FPGA's
- Hardware platform for VHDL / VERILOG / logic design courses
- Robotics
- High logic density applications at tight space constraints

2.3. Xilinx Spartan 3E XC3S500E_VQG100C Features:

Document [1] lists lots of goodies, here are the best facts:

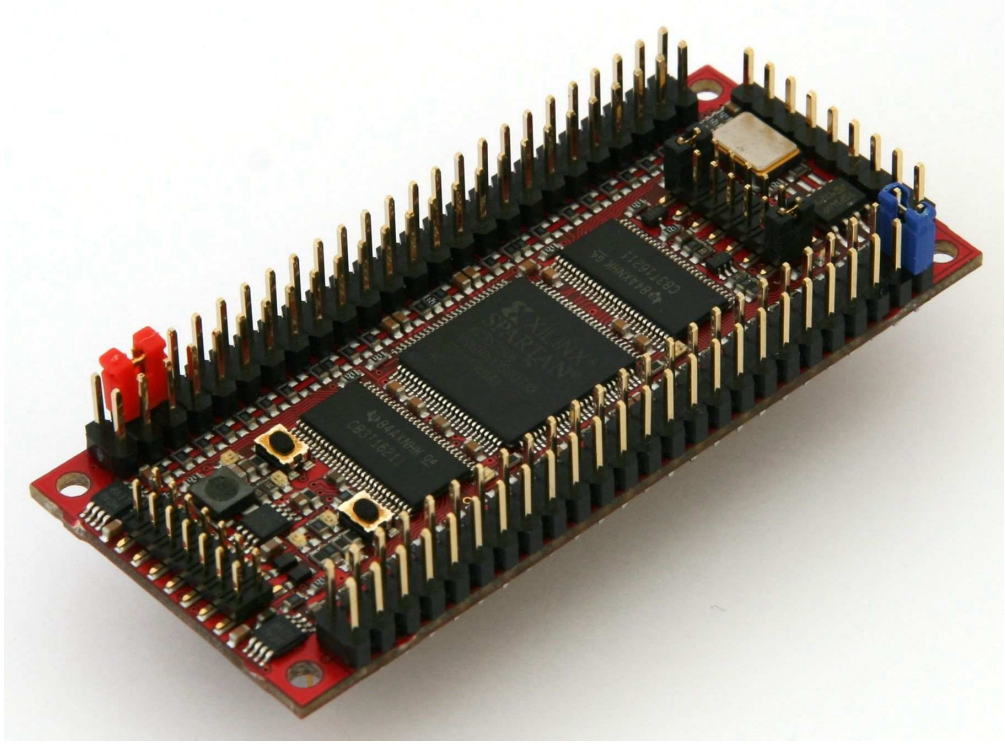
- Modern SRAM based 90nm 500k Gate low cost FPGA
- 9312 4-input function generators, 4656 can be RAM or dual ported RAM, or shift registers
- SPI FLASH can be used as configuration memory
- SelectRAM hierarchical memory, 20 x 18kbit Blockram, 73kbit distributed RAM
- 20 dedicated advanced multipliers 18x18
- 4 Digital Clock Managers, DCMs
- Lots of I/O standards, but GODIL supports LVCMOS33 and LVTTL only
- Wide multiplexers, fast look-ahead carry logic, 8 global clock nets, JTAG interface with user access
- Free powerful VHDL / VERILOG / schematics / simulation design software available (Webpack)
- Unlimited reprogrammability

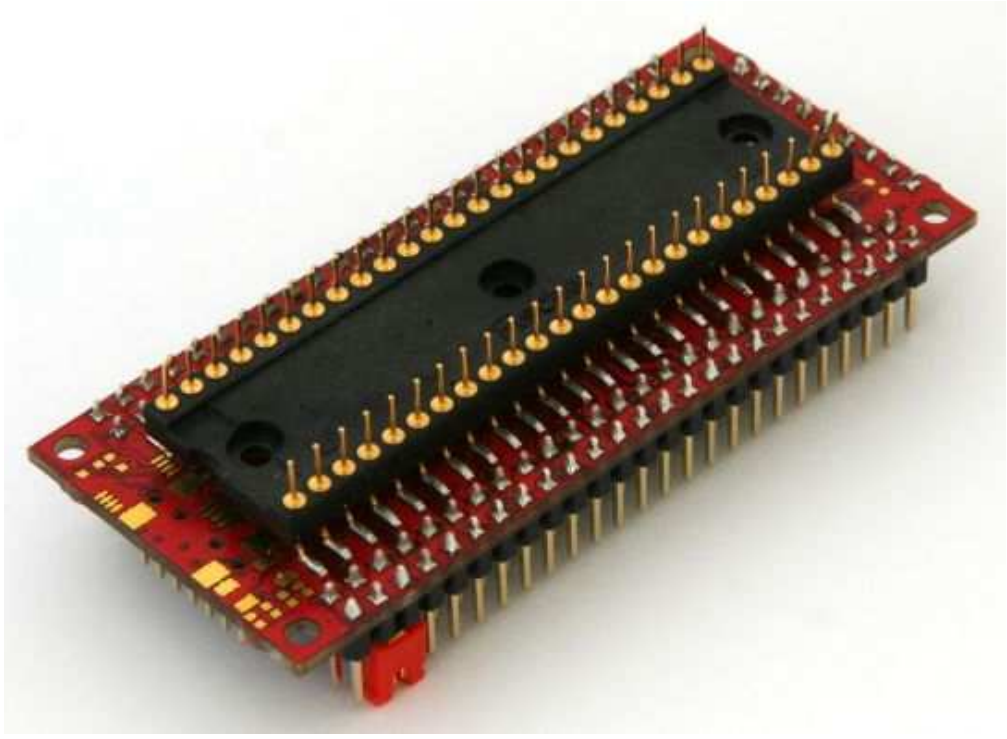
2.4. Xilinx Spartan 3E Disadvantages:

The following items are not relevant in most cases.However, they should be used as a checklist, to query wheather an application is affected.

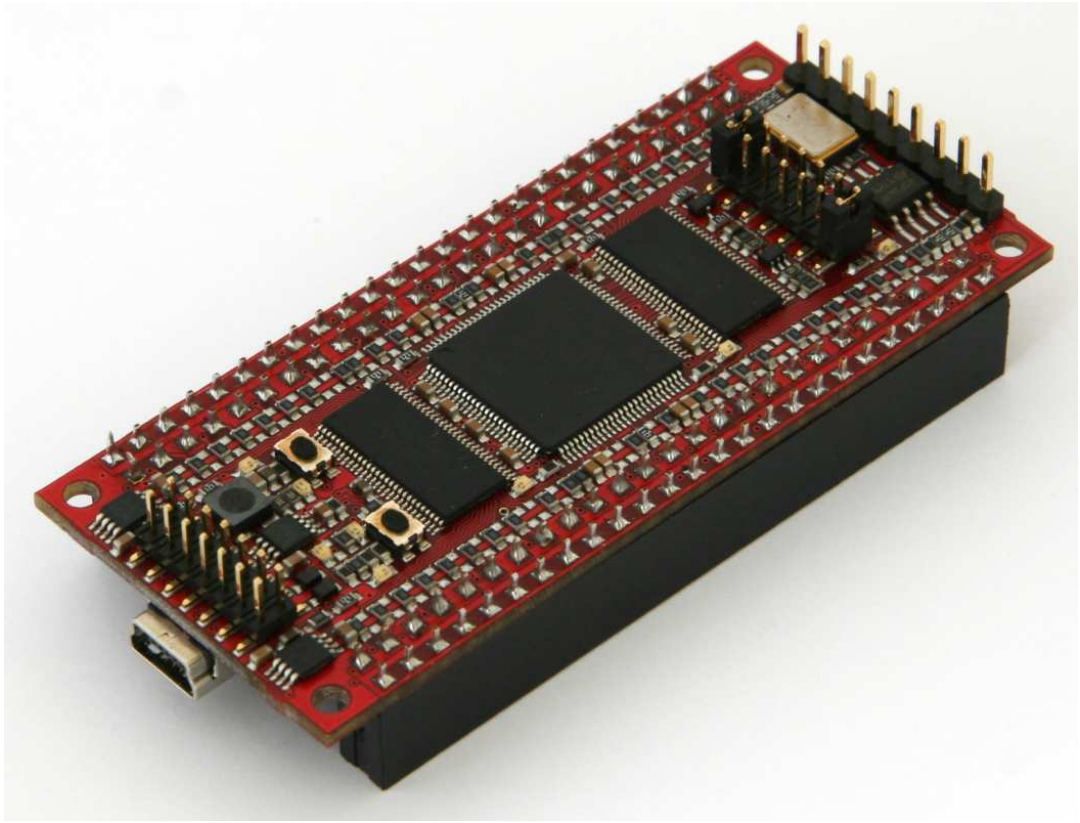
- No single chip solution, needs a configuration source like a platform FLASH
- 3 different supply voltages required: core voltage 1,2V, VCCAUX 2,5V, I/O voltage
- I/Os are not 5V tolerant
- High quiescent current, in the range of tens of milliamps for each of the supply voltages for XC3S500E
- Design is not protected against copyright theft, configuration bitstream can be recorded
- Lower performance FPGA compared to the luxury Virtex2 pro or Virtex4/5/6 FPGA's, especially not all LUTs have RAM / shift register capabilities
- DLLs in the DCM's have higher jitter than PLLs
- More modern Spartan 3A is less expensive, has more I/O features, but only 200k in VQG100 package

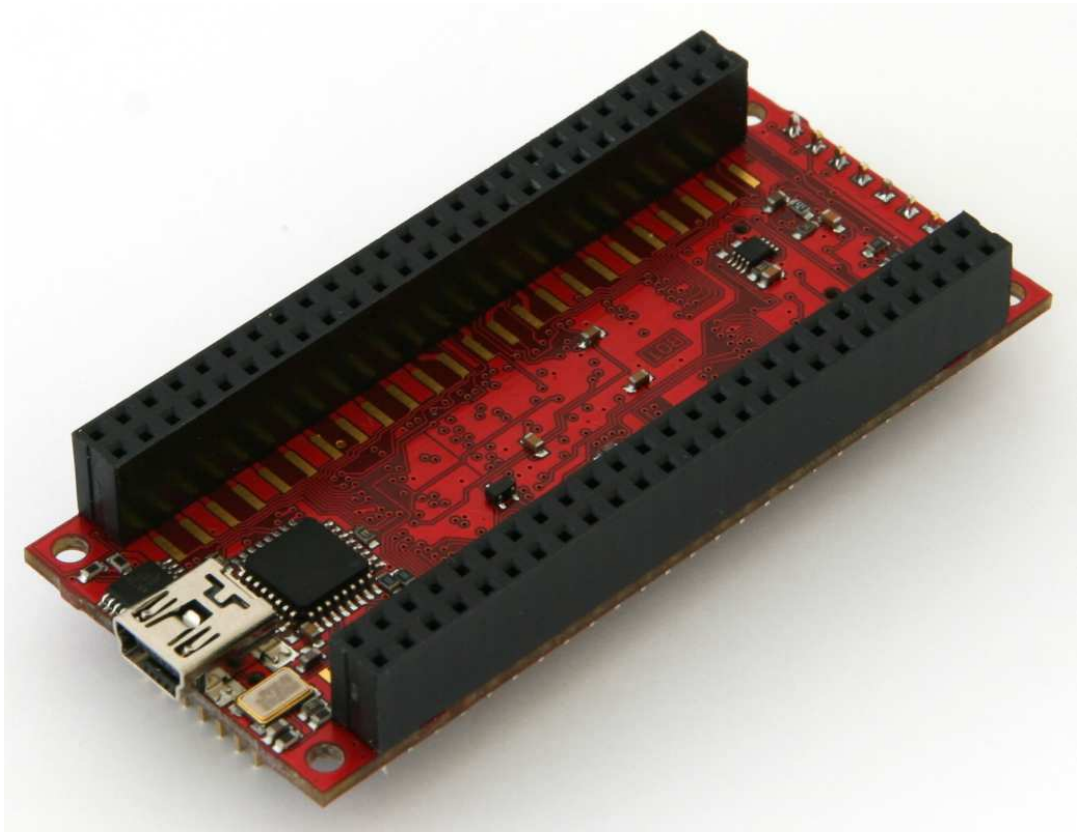
2.5. GODIL48 Board with DIL connector, Top And Bottom View.



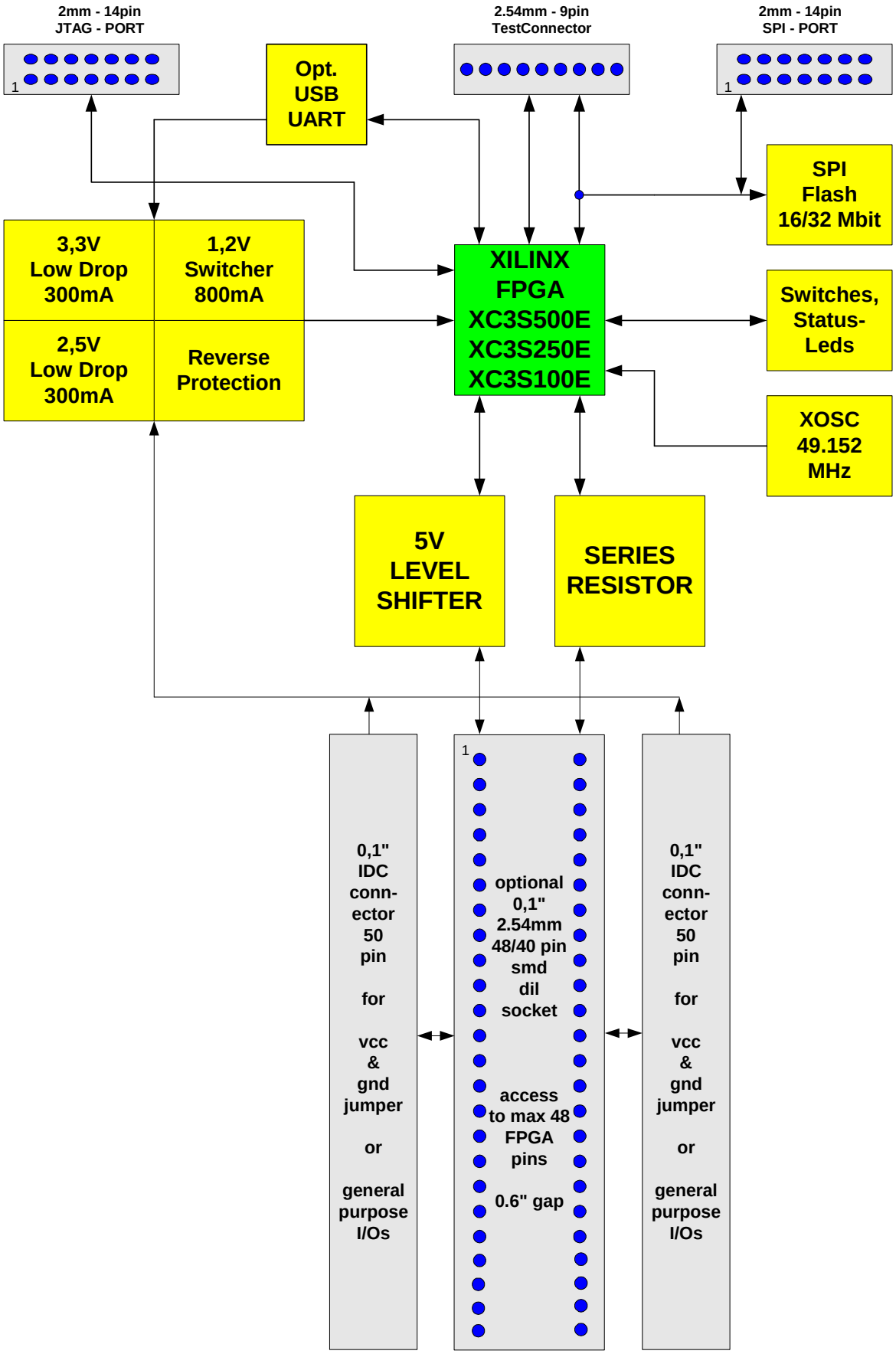


2.6. GODIL50 Board with IDC headers, Top And Bottom View.





3. GODIL Board Overview



3.1. I/O Distribution

48 I/Os of the Xilinx XC3S500E-4VQG100C FPGA are attached commonly to 2 different connector types, to a SMD DIL connector (CON1) with 48 or 40 pins, or to two 50 pin IDC headers (CON4G$1 and CON4G$2).

In a DIL application, beside the DIL connector also 2 IDC male headers must be soldered on the PCB top side.
These IDC connectors contain the 48 I/Os, 2 extra input only pins (C13 and D13, both are GCLK inputs) and in a regular grid GND and VCC connections.
With 2.54mm (0.1”) jumpers, GND and VCC must be plugged accordingly to the emulated DIL device, to supply the module with 3,5-5V.
There are two DIL connectors, a 48 pin connector and a 40 pin connector, which mechanically also allows for a USB option.

In an IDC only application, it is recommended to solder 2 female headers on the bottom side, no DIL connector must be assembled.

The I/Os of the FPGA are fed through level shifter devices 74CB3T16211, which makes the FPGA I/Os tolerant to input voltages up to 7V.
These level shifters can be bypassed through 0603 series resistors (all I/Os as a custom assembly or selected signals in the lab).

Please note, that the level shifter devices reduce the ability of the FPGA I/Os to source current, but sink current is not affected.

Some dual purpose I/Os are used on the test connector, see the mentioned chapter.

A crystal oscillator with an output frequency of 49,152MHz is connected to GCLK9 of the FPGA.
That oscillator must be enabled by a jumper on CON3 1-2.

There are 2 small tactile switches for user interaction, connected to FPGA input only pins.
SW1 is a high active signal which is also connected to the TUSB3410 DSR input.
SW2 is a low active signal which can be jumpered on CON3 for resetting the TUSB3410 or reconfiguation of the FPGA, see the SPI port chapter.

The following table show the function of the various status leds:

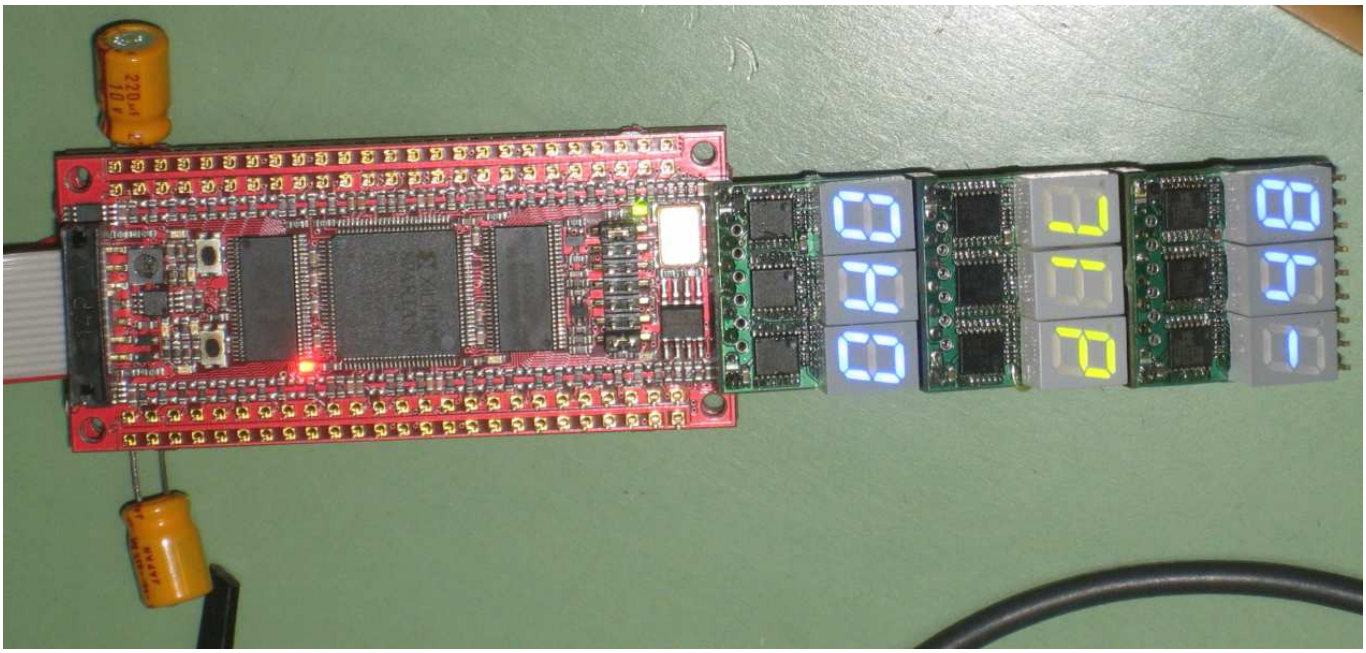
led#	colour	function
1	green	lights when the FPGA is configurd
2	red	lights when the FPGA is NOT configurd
3	red	SIN signals serial data sent from the FPGA to the TUSB3410, also available on non USB modules
4	red	SOUT signals serial data from the TUSB3410 to the FPGA, also available on non USB modules, but not usable
5	red	RTS signals serial handshake sent from the FPGA to the TUSB3410, also available on non USB modules
6	red	CTS signals serial handshake sent from the TUSB3410 to the FPGA, also available on non USB modules, but not usable
7	red	DTR signals FPGA reconfiguration sent from the TUSB3410 to the FPGA, also available on non USB modules, but not usable
8	green	VS2 is a free signal on the FPGA, rarely used for I2C eeprom programming with the USB option
9	red	CSO signals access of the SPI FLASH, can be during configuration or by FPGA user activity on the I/O pin.
10	red	normally not mounted
11	red	normally not mounted

As a future option, a full speed USB interface is available on the bottom side of the board.

3.2. Test connector

7 I/Os are available to the front side test connector CON4G$3 for debugging purposes.
These I/Os are dual purpose pins, in the FPGA configuration phase, no active low input must be applied to any pin.

The test connector is primarily intended for probes to an oscilloscope or logic analyzer. But since a power supply is also provided on the connector, it is ideally suited for small hardware extensions or debug modules like the 3-digit OHO_DY1 display module.



3.3. JTAG Port

The FPGA is the only member in the JTAG chain connected to CON2.

The FPGA normally configures from the SPI FLASH devices M25P16 or M25P32 (for debugging JTAG configuration is always also possible).
The SPI Flash can be programmed via its dedicated programming header CON3.
However indirect programming via the JTAG chain with ISE10.1 (and newer SW) is recommended.

The configuration status of the FPGA is shown by the red status led2 and the green status led1.
If the FPGA is not configured, red led2 is lit, and the green led1 is dark.
If the FPGA is configured, green led1 is lit, and the red led2 is dark.

The FPGA JTAG chain is routed to the Xilinx standard 2mm 14pin JTAG port connector CON2 by serial resistors, enabling JTAG programming with 3,3V voltage levels.

The 2mm connector is supported by the OHO GOPLCP, and the Xilinx products parallel cable IV, and platform USB cables, see [2], [3] and [4].

Pressing SW1 before powering the GODIL module skips the configuration process, and the FPGA awaits configuring from the JTAG port only.

The JTAG connector has a jumper feature on pins 1-2, which enables programming of the I2C eeprom for the TUSB3410 USB interface with a special FPGA design.

Pins 12 and 14 of the connector allows measurement of the internal voltages V1V2 and V2V5 only if the USB option is assmbled.

3.4. SPI Port

The onboard SPI Flash M25P16 or M25P32 can be programmed directly with Software versions prior to ISE10.1 via the SPI port CON3.

When using the Xilinx USB-II programmer, insure that pin13 is grounded, which holds the FPGA in a reset state during programming.

When the port is not used, some jumper positions at CON3 are used for the following module features:

- CON3 pin1-2 enables the onboard crystal oscillator
- CON3 pin13-14 allows SW2 to reconfigure the FPGA
- CON3 pin12-14 allows SW2 to reset the TUSB3410
- CON3 pin11-12 always resets the TUSB3410

Avoid using other jumper positions, otherwise the module may not be able to configure from the SPI FLASH.

3.5. Power Supply

The module can be powered with supplies from 3.5 to 5.5 volts, since core and auxiliary voltages are generated with on-board regulators.

An onboard switching voltage regulator produces the FPGA core voltage of 1,2V.
The regulator [6] can source up to 800mA.
Another 2 low drop regulators generate the VCCAUX voltage of 2,5V and the VCCO voltage of 3,3V, sourcing up to 300mA [5].

The module has a simple schottky diode as a protection against reverse insertion, or reverse power connection
Even so, care should be taken when plugging the module.

ATTENTION !!!
Please note, that a voltage above 6V on the module GND and VCC pins will destroy the voltage regulators on the module !!!
Especially the switching regulator is sensitive to overvoltage. Therefore, the maximum of 5,5V module supply voltage must never be exceeded.

4. About GODIL I/O Voltage Levels

The Spartan3E FPGA series offer a broad variety of I/O voltage standards.
However on the GODIL module, only the LVCMOS33 and LVTTL standards are supported.
These standards are required for the level shifters [7] for conversion of 5V TTL levels as well as 5V CMOS levels.
These level shifters work bidirectionally without the need of controlling their direction.

Please note, that the level shifter devices reduces the ability of the FPGA I/Os to source current, sink current is not affected.
The level shifters introduce a delay of 0,25ns maximum.

Further on, the shifters do not clamp the outputs to their VCC of 3,3V.
They can be lifted up by pullups to a maximum of 7V.

The GODIL module I/Os have 1,5k pullups to 5V.

The level shifters can be bypassed by soldering 0603 resistors in parallel to the shifter for any I/O, if higher source currents are needed.

5. Detailed XC3S500E-4VQG100C FPGA Pinout Table

Pin	FPGA pin function	(Schema net name) routed to	UCF port name	Comment
1	PROG_B	(prog) CON3 pin13	--	FPGA configuration reset signal, active low,, can be driven by the TUSB3410 or SW2 by jumper
2	I/O_L01P_3	(F02) IC3 pin54	pin<40>	Connection to the 48 pin DIL plug to pin40 via level shifter
3	I/O_L01N_3	(F03) IC3 pin53	pin<39>	Connection to the 48 pin DIL plug to pin39 via level shifter
4	I/O_L02P_3	(F04) IC3 pin52	pin<41>	Connection to the 48 pin DIL plug to pin41 via level shifter
5	I/O_L02N_3 VREF3	(F05) IC3 pin51	pin<42>	Connection to the 48 pin DIL plug to pin42 via level shifter
6	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
7	GND	GND	--	Connection to the GND Layer of the PCB
8	VCCO_3	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
9	I/O_L03P_3 LHCLK0	(F09) IC3 pin47	pin<44>	Connection to the 48 pin DIL plug to pin44 via level shifter
10	I/O_L03N_3 LHCLK1	(F10) IC3 pin46	pin<45>	Connection to the 48 pin DIL plug to pin45 via level shifter
11	I/O_L04P_3 LHCLK2	(F11) IC3 pin45	pin<46>	Connection to the 48 pin DIL plug to pin46 via level shifter
12	I/O_L04N_3 LHCLK3	(F12) IC3 pin44	pin<47>	Connection to the 48 pin DIL plug to pin47 via level shifter
13	IP	(SOUT) TUSB3410	sout	TUSB3410 serial data output
14	GND	GND	--	Connection to the GND Layer of the PCB
15	I/O_L04N_3 LHCLK4	(F15) IC3 pin41	pin<2>	Connection to the 48 pin DIL plug to pin2 via level shifter
16	I/O_L04N_3 LHCLK5	(F16) IC3 pin40	pin<3>	Connection to the 48 pin DIL plug to pin3 via level shifter
17	I/O_L04N_3 LHCLK6	(F17) IC3 pin36	pin<6>	Connection to the 48 pin DIL plug to pin6 via level shifter
18	I/O_L04N_3 LHCLK7	(F18) IC3 pin37	pin<5>	Connection to the 48 pin DIL plug to pin5 via level shifter
19	GND	GND	--	Connection to the GND Layer of the PCB
20	VCCO_3	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
21	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
22	I/O_L07P_3	(F22) IC3 pin33	pin<8>	Connection to the 48 pin DIL plug to pin8 via level shifter
23	I/O_L07N_3	(F23) IC3 pin32	pin<9>	Connection to the 48 pin DIL plug to pin9 via level shifter
24	I/O_L01P_2 CSO_B	(CSO) IC4 pin1	cso	FPGA SPI configuration memory chip select
25	I/O_L01N_2 INIT_B	(CTS) IC6 pin13 LED6	cts	CLEAR TO SEND CTS to TUSB3410, handskae signal also controls red led6
26	I/O_L02P_2 DOUT	(DOUT) IC3 pin42	pin<1>	Connection to the 48 pin DIL plug to pin1 via level shifter
27	I/O_L01N_2 MOSI	(MOSI) SW1	tmosi	SPI Flash MOSI Pin E4 testconnector over 330 ohms

28	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
29	GND	GND	--	Connection to the GND Layer of the PCB
30	IP VREF2	(RTS) IC6 pin20 led5	rts	TUSB3410 output Ready to Send handshake signal also controls red led5
31	VCCO_2	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
32	I/O_L03P_2 GCLK12	(F32) IC3 pin29	pin<11>	Connection to the 48 pin DIL plug to pin11 via level shifter
33	I/O_L03N_2 GCLK13	(F33) IC3 pin30	pin<10>	Connection to the 48 pin DIL plug to pin10 via level shifter
34	I/O	(F34) IC3 pin31	pin<12>	Connection to the 48 pin DIL plug to pin12 via level shifter
35	I/O_L04P_2 GCLK14	(F35) IC1 pin52	pin<16>	Connection to the 48 pin DIL plug to pin16 via level shifter
36	I/O_L07N_3 GCLK15	(F36) IC1 pin53	pin<15>	Connection to the 48 pin DIL plug to pin15 via level shifter
37	GND	GND	--	Connection to the GND Layer of the PCB
38	IP_L05P_2 GCLK0	(F38) CON4G$1 pin49	c13	external input only at connector C13, PIN<49> via series resistor of 120ohms
39	IP_L05P_2 GCLK1 M2	(SW1) IC6 pin14	sw1	switch 1, high active also triggers DSR on TUSB3410 also allows FPGA JTAG configuration only when depressed before applying power to the module
40	I/O_L06P_2 GCLK2	(F40) IC1 pin46	pin<13>	Connection to the 48 pin DIL plug to pin13 via level shifter
41	I/O_L06N_2 GCLK3	(F41) IC1 pin54	pin<14>	Connection to the 48 pin DIL plug to pin14 via level shifter
42	I/O_L06N_2 M1	(M1)	tm1	M1 configuration mode pin, driven low during configuration by D1 / T1G$2 Pin E7 testconnector over 330 ohms
43	I/O_L07P_2 M0	(SIN) IC6 pin17	sin	M0 configuration mode pin, driven high during configuration by led pullup TUSB3410 serial data input also controls led3 red
44	I/O_L07N_2 DIN	(DIN) IC4 pin2	tdin	SPI FLASH data out Pin E5 testconnector over 330 ohms
45	VCCO_2	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
46	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
47	I/O_L08P_2 VS2	(VS2) IC10 pin2 led8	vs2	TUSB3410 I2C connection over analog switch also controls led8 green
48	I/O_L08N_2 VS1	(VS1) IC10 pin6	tvs1	TUSB3410 I2C connection over analog switch Pin E2 testconnector over 120ohms
49	I/O_L09P_2 VS0	(VS0)	tvs0	Pin E3 testconnector over 120ohms
50	I/O_L09N_2 CCLK	(CCLK) IC4 pin6	tcclk	SPI FLASH configuration clock Pin E6 testconnector over 330ohms
51	DONE	(DONE)	--	FPGA configuration ready strobe, 1 = fpga configured
52	GND	GND	--	Connection to the GND Layer of the PCB
53	I/O_L01P_1	(F53) IC1 pin51	pin<17>	Connection to the 48 pin DIL plug to pin17 via level shifter
54	I/O_L01N_1	(F54) IC1 pin50	pin<18>	Connection to the 48 pin DIL plug to pin18 via level shifter

55	VCCO_1	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
56	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
57	I/O_L02P_1	(F57) IC1 pin48	pin<19>	Connection to the 48 pin DIL plug to pin19 via level shifter
58	I/O_L02N_1	(F58) IC1 pin47	pin<20>	Connection to the 48 pin DIL plug to pin20 via level shifter
59	GND	GND	--	Connection to the GND Layer of the PCB
60	I/O_L03P_1 RHCLK0	(F60) IC1 pin45	pin<21>	Connection to the 48 pin DIL plug to pin21 via level shifter
61	I/O_L03N_1 RHCLK1	(F61) IC1 pin44	pin<22>	Connection to the 48 pin DIL plug to pin22 via level shifter
62	I/O_L04P_1 RHCLK2	(F62) IC1 pin43	pin<23>	Connection to the 48 pin DIL plug to pin23 via level shifter
63	I/O_L04N_1 RHCLK3	(F63) IC1 pin42	pin<24>	Connection to the 48 pin DIL plug to pin24 via level shifter
64	GND	GND	--	Connection to the GND Layer of the PCB
65	I/O_L05P_1 RHCLK4	(F65) IC1 pin41	pin<25>	Connection to the 48 pin DIL plug to pin25 via level shifter
66	I/O_L05N_1 RHCLK5	(F66) IC1 pin40	pin<26>	Connection to the 48 pin DIL plug to pin26 via level shifter
67	I/O_L06P_1 RHCLK6	(F67) IC1 pin39	pin<27>	Connection to the 48 pin DIL plug to pin27 via level shifter
68	I/O_L06N_1 RHCLK7	(F68) IC1 pin37	pin<28>	Connection to the 48 pin DIL plug to pin28 via level shifter
69	IP VREF1	(SW2) CON3 pin14	sw2	switch 2, low active
70	I/O_L07P_1	(F70) IC1 pin36	pin<29>	Connection to the 48 pin DIL plug to pin29 via level shifter
71	I/O_L07N_1	(F71) IC1 pin35	pin<30>	Connection to the 48 pin DIL plug to pin30 via level shifter
72	GND	GND	--	Connection to the GND Layer of the PCB
73	VCCO_1	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
74	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
75	TMS	(FTMS) CON2 pin4 via 120ohms	--	FPGA JTAG chain JTAG TMS via serial resistor to support 3,3V download adapter
76	TDO	(FTDO) CON2 pin8	--	FPGA JTAG chain
77	TCK	(FTCK) CON2 pin6 via 120ohms	--	FPGA JTAG chain JTAG TCK via serial resistor to support 3,3V download adapter
78	I/O_L01P_0	(F78) IC1 pin29	pin<34>	Connection to the 48 pin DIL plug to pin34 via level shifter
79	I/O_L01N_0	(F79) IC1 pin30	pin<35>	Connection to the 48 pin DIL plug to pin35 via level shifter
80	VCCINT	(VCC1V2)	--	Internal core Voltage 1,2V
81	GND	GND	--	Connection to the GND Layer of the PCB
82	VCCO_0	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
83	I/O_L02P_0 GCLK4	(F83) IC1 pin31	pin<33>	Connection to the 48 pin DIL plug to pin33 via level shifter
84	I/O_L02N_0 GCLK5	(F84) IC1 pin32	pin<32>	Connection to the 48 pin DIL plug to pin32 via level shifter
85	I/O_L03P_0 GCLK6	(F85) IC1 pin33	pin<36>	Connection to the 48 pin DIL plug to pin36 via level shifter
86	I/O_L03N_0	(F86)	pin<31>	Connection to the 48 pin DIL plug to pin31 via level shifter

	GCLK7	IC1 pin34		
87	GND	GND	--	Connection to the GND Layer of the PCB
88	I/O_L04P_0 GCLK8	(F88) CON4G$2 pin50	d13	external input only at connector D13, PIN<50> via series resistor of 120ohms
89	I/O_L04N_0 GCLK9	(F89)	m49	XOSC crystal oscillator input
90	I/O_L05P_0 GCLK10	(F90) IC3 pin48	pin<43>	Connection to the 48 pin DIL plug to pin43 via level shifter
91	I/O_L05N_0 GCLK11	(F91) IC3 pin43	pin<48>	Connection to the 48 pin DIL plug to pin48 via level shifter
92	I/O	(F92) IC3 pin50	pin<37>	Connection to the 48 pin DIL plug to pin37 via level shifter
93	GND	GND	--	Connection to the GND Layer of the PCB
94	I/O_L06P_0	(F94) IC3 pin35	pin<7>	Connection to the 48 pin DIL plug to pin7 via level shifter
95	I/O_L06N_0	(F95) IC3 pin39	pin<4>	Connection to the 48 pin DIL plug to pin4 via level shifter
96	VCCAUX	(VCC2V5)	--	VCCAUX must be 2,5V
97	VCCO_0	(VCC3V3)	--	LVCMOS33/LVTTL I/O Voltage 3,3V
98	I/O_L07P_0 GCLK2	(F98) IC3 pin34	pin<38>	Connection to the 48 pin DIL plug to pin38 via level shifter
99	I/O_L07N_0 HSWAP	(HSW)	thsw	HSWAP configuration mode pin, driven low during configuration by D1 / T1G$2 Pin E8 testconnector over 330 ohms
100	TDI	(FTDI) CON2 pin10 via 120ohms	--	FPGA JTAG chain JTAG TDI via serial resistor to support 3,3V download adapter

6. CON4G$1 Left Header Connector Pinout Table

FPGA pin	Direction	Signal name 48,(40pins)	Pin row C	Pin row A	Signal name 48,(40pins)	Direction	FPGA pin
P26	I/O	pin<1>	C1	A1	GND	-	-
-	-	V+	C2	A2	pin<2>	I/O	P15
P16	I/O	pin<3> (pin<1>)	C3	A3	GND	-	-
-	-	V+	C4	A4	pin<4> (pin<2>)	I/O	P95
P18	I/O	pin<5> (pin<3>)	C5	A5	GND	-	-
-	-	V+	C6	A6	pin<6> (pin<4>)	I/O	P17
P94	I/O	pin<7> (pin<5>)	C7	A7	GND	-	-
-	-	V+	C8	A8	pin<8> (pin<6>)	I/O	P22
P23	I/O	pin<9> (pin<7>)	C9	A9	GND	-	-
-	-	V+	C10	A10	pin<10> (pin<8>)	I/O	P33
P32	I/O	pin<11> (pin<9>)	C11	A11	GND	-	-
-	-	V+	C12	A12	pin<12> (pin<10>)	I/O	P34
P38	Input only	pin<49> (not on DIL)	C13	A13	GND	-	-
-	-	V+	C14	A14	pin<13> (pin<11>)	I/O	P40
P41	I/O	pin<14> (pin<12>)	C15	A15	GND	-	-
-	-	V+	C16	A16	pin<15> (pin<13>)	I/O	P36
P35	I/O	pin<16> (pin<14>)	C17	A17	GND	-	-
-	-	V+	C18	A18	pin<17> (pin<15>)	I/O	P53
P54	I/O	pin<18> (pin<16>)	C19	A19	GND	-	-
-	-	V+	C20	A20	pin<19> (pin<17>)	I/O	P57
P58	I/O	pin<20> (pin<18>)	C21	A21	GND	-	-
-	-	V+	C22	A22	pin<21> (pin<19>)	I/O	P60
P61	I/O	pin<22> (pin<20>)	C23	A23	GND	-	-
-	-	V+	C24	A24	pin<23>	I/O	P62
P63	I/O	pin<24>	C25	A25	GND	-	-

As an example, to put VSS (GND) to a GODIL40 module on pin 20, place a jumper between header pins [C23 and A23].

7. CON4G$2 Right Header Connector Pinout Table

FPGA pin	Direction	Signal name 48,(40pins)	Pin row B	Pin row D	Signal name 48,(40pins)	Direction	FPGA pin
-	-	GND	B1	D1	pin<48>	I/O	P91
P12	I/O	pin<47>	B2	D2	V+	-	-
-	-	GND	B3	D3	pin<46> (pin<40>)	I/O	P11
P10	I/O	pin<45> (pin<39>)	B4	D4	V+	-	-
-	-	GND	B5	D5	pin<44> (pin<38>)	I/O	P9
P90	I/O	pin<43> (pin<37>)	B6	D6	V+	-	-
-	-	GND	B7	D7	pin<42> (pin<36>)	I/O	P5
P4	I/O	pin<41> (pin<35>)	B8	D8	V+	-	-
-	-	GND	B9	D9	pin<40> (pin<34>)	I/O	P2
P3	I/O	pin<39> (pin<33>)	B10	D10	V+	-	-
-	-	GND	B11	D11	pin<38> (pin<32>)	I/O	P98
P92	I/O	pin<37> (pin<31>)	B12	D12	V+	-	-
-	-	GND	B13	D13	pin<50> (not on DIL)	Input only	P88
P85	I/O	pin<36> (pin<30>)	B14	D14	V+	-	-
-	-	GND	B15	D15	pin<35> (pin<29>)	I/O	P79
P78	I/O	pin<34> (pin<28>)	B16	D16	V+	-	-
-	-	GND	B17	D17	pin<33> (pin<27>)	I/O	P83
P84	I/O	pin<32> (pin<26>)	B18	D18	V+	-	-
-	-	GND	B19	D19	pin<31> (pin<25>)	I/O	P86
P71	I/O	pin<30> (pin<24>)	B20	D20	V+	-	-
-	-	GND	B21	D21	pin<29> (pin<23>)	I/O	P70
P68	I/O	pin<28> (pin<22>)	B22	D22	V+	-	-
-	-	GND	B23	D23	pin<27> (pin<21>)	I/O	P67
P66	I/O	pin<26>	B24	D24	V+	-	-
-	-	GND	B25	D25	pin<25>	I/O	P65

As an example, to put VCC (+5V) to a GODIL40 module on pin 40, place a jumper between header pins [D2 and D3] or [D3 and D4].

8. CON4G$3 Test Connector Pinout Table

Pin	FPGA pin function *	(Schema net name) routed to	UCF port name **	Comment
E1	GND	GND	--	Power ground plane connection
E2	I/O_L08N_2 VS1	(VS1) IC10 pin6	tvs1	TUSB3410 I2C connection over analog switch Pin E2 testconnector over 120ohms
E3	I/O_L09P_2 VS0	(VS0)	tvs0	Pin E3 testconnector over 120ohms
E4	I/O_L01N_2 MOSI	(MOSI) SW1	tmosi	SPI Flash MOSI Pin E4 testconnector over 330 ohms
E5	I/O_L07N_2 DIN	(DIN) IC4 pin2	tdin	SPI FLASH data out Pin E5 testconnector over 330 ohms
E6	I/O_L09N_2 CCLK	(CCLK) IC4 pin6	tcclk	SPI FLASH configuration clock Pin E6 testconnector over 330ohms
E7	I/O_L06N_2 M1	(M1)	tm1	M1 configuration mode pin, driven low during configuration by D1 / T1G$2 Pin E7 testconnector over 330 ohms
E8	I/O_L07N_0 HSWAP	(HSW)	thsw	HSWAP configuration mode pin, driven low during configuration by D1 / T1G$2 Pin E8 testconnector over 330 ohms
E9	VIN	(VIN)	--	5V input voltage protected by a 0603 0ohm resistor

9. CON1 DIL48 Connector Pinout Table

Pin	FPGA pin function	(Schema net name) routed to	UCF port name	Comment
1	I/O_L02P_2 DOUT	(DOUT) IC3 pin42	pin<1>	Connection to the 48 pin DIL plug to pin1 via level shifter
2	I/O_L04N_3 LHCLK4	(F15) IC3 pin41	pin<2>	Connection to the 48 pin DIL plug to pin2 via level shifter
3	I/O_L04N_3 LHCLK5	(F16) IC3 pin40	pin<3>	Connection to the 48 pin DIL plug to pin3 via level shifter
4	I/O_L06N_0	(F95) IC3 pin39	pin<4>	Connection to the 48 pin DIL plug to pin4 via level shifter
5	I/O_L04N_3 LHCLK7	(F18) IC3 pin37	pin<5>	Connection to the 48 pin DIL plug to pin5 via level shifter
6	I/O_L04N_3 LHCLK6	(F17) IC3 pin36	pin<6>	Connection to the 48 pin DIL plug to pin6 via level shifter
7	I/O_L06P_0	(F94) IC3 pin35	pin<7>	Connection to the 48 pin DIL plug to pin7 via level shifter
8	I/O_L07P_3	(F22) IC3 pin33	pin<8>	Connection to the 48 pin DIL plug to pin8 via level shifter
9	I/O_L07N_3	(F23) IC3 pin32	pin<9>	Connection to the 48 pin DIL plug to pin9 via level shifter
10	I/O_L03N_2 GCLK13	(F33) IC3 pin30	pin<10>	Connection to the 48 pin DIL plug to pin10 via level shifter
11	I/O_L03P_2 GCLK12	(F32) IC3 pin29	pin<11>	Connection to the 48 pin DIL plug to pin11 via level shifter
12	I/O	(F34) IC3 pin31	pin<12>	Connection to the 48 pin DIL plug to pin12 via level shifter
13	I/O_L06P_2 GCLK2	(F40) IC1 pin46	pin<13>	Connection to the 48 pin DIL plug to pin13 via level shifter
14	I/O_L06N_2 GCLK3	(F41) IC1 pin54	pin<14>	Connection to the 48 pin DIL plug to pin14 via level shifter
15	I/O_L07N_3 GCLK15	(F36) IC1 pin53	pin<15>	Connection to the 48 pin DIL plug to pin15 via level shifter
16	I/O_L04P_2 GCLK14	(F35) IC1 pin52	pin<16>	Connection to the 48 pin DIL plug to pin16 via level shifter
17	I/O_L01P_1	(F53) IC1 pin51	pin<17>	Connection to the 48 pin DIL plug to pin17 via level shifter
18	I/O_L01N_1	(F54) IC1 pin50	pin<18>	Connection to the 48 pin DIL plug to pin18 via level shifter
19	I/O_L02P_1	(F57) IC1 pin48	pin<19>	Connection to the 48 pin DIL plug to pin19 via level shifter
20	I/O_L02N_1	(F58) IC1 pin47	pin<20>	Connection to the 48 pin DIL plug to pin20 via level shifter
21	I/O_L03P_1 RHCLK0	(F60) IC1 pin45	pin<21>	Connection to the 48 pin DIL plug to pin21 via level shifter
22	I/O_L03N_1 RHCLK1	(F61) IC1 pin44	pin<22>	Connection to the 48 pin DIL plug to pin22 via level shifter
23	I/O_L04P_1 RHCLK2	(F62) IC1 pin43	pin<23>	Connection to the 48 pin DIL plug to pin23 via level shifter
24	I/O_L04N_1 RHCLK3	(F63) IC1 pin42	pin<24>	Connection to the 48 pin DIL plug to pin24 via level shifter

25	I/O_L05P_1 RHCLK4	(F65) IC1 pin41	pin<25>	Connection to the 48 pin DIL plug to pin25 via level shifter
26	I/O_L05N_1 RHCLK5	(F66) IC1 pin40	pin<26>	Connection to the 48 pin DIL plug to pin26 via level shifter
27	I/O_L06P_1 RHCLK6	(F67) IC1 pin39	pin<27>	Connection to the 48 pin DIL plug to pin27 via level shifter
28	I/O_L06N_1 RHCLK7	(F68) IC1 pin37	pin<28>	Connection to the 48 pin DIL plug to pin28 via level shifter
29	I/O_L07P_1	(F70) IC1 pin36	pin<29>	Connection to the 48 pin DIL plug to pin29 via level shifter
30	I/O_L07N_1	(F71) IC1 pin35	pin<30>	Connection to the 48 pin DIL plug to pin30 via level shifter
31	I/O_L03N_0 GCLK7	(F86) IC1 pin34	pin<31>	Connection to the 48 pin DIL plug to pin31 via level shifter
32	I/O_L02N_0 GCLK5	(F84) IC1 pin32	pin<32>	Connection to the 48 pin DIL plug to pin32 via level shifter
33	I/O_L02P_0 GCLK4	(F83) IC1 pin31	pin<33>	Connection to the 48 pin DIL plug to pin33 via level shifter
34	I/O_L01P_0	(F78) IC1 pin29	pin<34>	Connection to the 48 pin DIL plug to pin34 via level shifter
35	I/O_L01N_0	(F79) IC1 pin30	pin<35>	Connection to the 48 pin DIL plug to pin35 via level shifter
36	I/O_L03P_0 GCLK6	(F85) IC1 pin33	pin<36>	Connection to the 48 pin DIL plug to pin36 via level shifter
37	I/O	(F92) IC3 pin50	pin<37>	Connection to the 48 pin DIL plug to pin37 via level shifter
38	I/O_L07P_0 GCLK2	(F98) IC3 pin34	pin<38>	Connection to the 48 pin DIL plug to pin38 via level shifter
39	I/O_L01N_3	(F03) IC3 pin53	pin<39>	Connection to the 48 pin DIL plug to pin39 via level shifter
40	I/O_L01P_3	(F02) IC3 pin54	pin<40>	Connection to the 48 pin DIL plug to pin40 via level shifter
41	I/O_L02P_3	(F04) IC3 pin52	pin<41>	Connection to the 48 pin DIL plug to pin41 via level shifter
42	I/O_L02N_3 VREF3	(F05) IC3 pin51	pin<42>	Connection to the 48 pin DIL plug to pin42 via level shifter
43	I/O_L05P_0 GCLK10	(F90) IC3 pin48	pin<43>	Connection to the 48 pin DIL plug to pin43 via level shifter
44	I/O_L03P_3 LHCLK0	(F09) IC3 pin47	pin<44>	Connection to the 48 pin DIL plug to pin44 via level shifter
45	I/O_L03N_3 LHCLK1	(F10) IC3 pin46	pin<45>	Connection to the 48 pin DIL plug to pin45 via level shifter
46	I/O_L04P_3 LHCLK2	(F11) IC3 pin45	pin<46>	Connection to the 48 pin DIL plug to pin46 via level shifter
47	I/O_L04N_3 LHCLK3	(F12) IC3 pin44	pin<47>	Connection to the 48 pin DIL plug to pin47 via level shifter
48	I/O_L05N_0 GCLK11	(F91) IC3 pin43	pin<48>	Connection to the 48 pin DIL plug to pin48 via level shifter

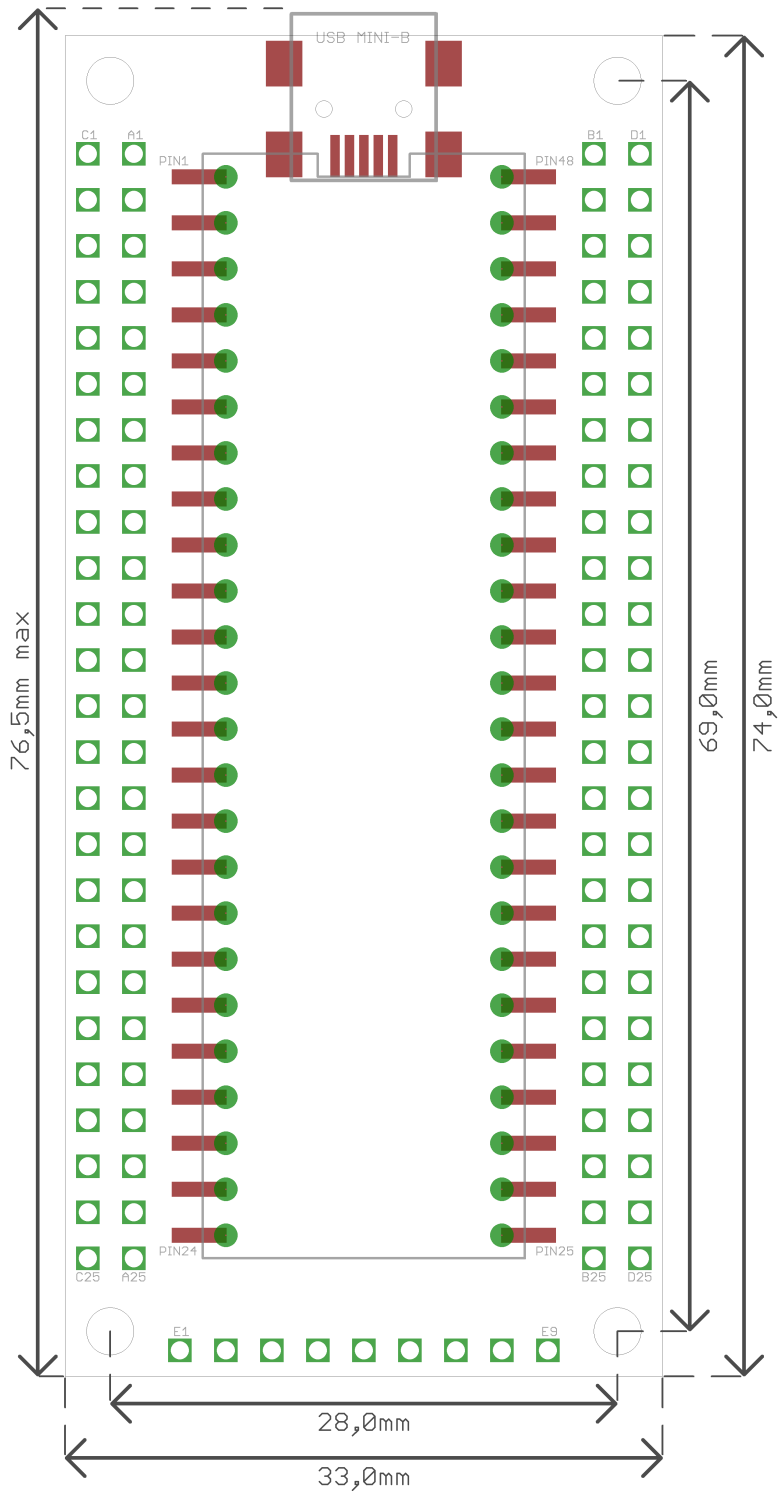
10. CON1 DIL40 Connector Pinout Table

Pin	FPGA pin function	(Schema net name) routed to	UCF port name	Comment
1	I/O_L04N_3 LHCLK5	(F16) IC3 pin40	pin<1>	Connection to the 40 pin DIL plug to pin3 via level shifter
2	I/O_L06N_0	(F95) IC3 pin39	pin<2>	Connection to the 40 pin DIL plug to pin4 via level shifter
3	I/O_L04N_3 LHCLK7	(F18) IC3 pin37	pin<3>	Connection to the 40 pin DIL plug to pin5 via level shifter
4	I/O_L04N_3 LHCLK6	(F17) IC3 pin36	pin<4>	Connection to the 40 pin DIL plug to pin6 via level shifter
5	I/O_L06P_0	(F94) IC3 pin35	pin<5>	Connection to the 40 pin DIL plug to pin7 via level shifter
6	I/O_L07P_3	(F22) IC3 pin33	pin<6>	Connection to the 40 pin DIL plug to pin8 via level shifter
7	I/O_L07N_3	(F23) IC3 pin32	pin<7>	Connection to the 40 pin DIL plug to pin9 via level shifter
8	I/O_L03N_2 GCLK13	(F33) IC3 pin30	pin<8>	Connection to the 40 pin DIL plug to pin10 via level shifter
9	I/O_L03P_2 GCLK12	(F32) IC3 pin29	pin<9>	Connection to the 40 pin DIL plug to pin11 via level shifter
10	I/O	(F34) IC3 pin31	pin<10>	Connection to the 40 pin DIL plug to pin12 via level shifter
11	I/O_L06P_2 GCLK2	(F40) IC1 pin46	pin<11>	Connection to the 40 pin DIL plug to pin13 via level shifter
12	I/O_L06N_2 GCLK3	(F41) IC1 pin54	pin<12>	Connection to the 40 pin DIL plug to pin14 via level shifter
13	I/O_L07N_3 GCLK15	(F36) IC1 pin53	pin<13>	Connection to the 40 pin DIL plug to pin15 via level shifter
14	I/O_L04P_2 GCLK14	(F35) IC1 pin52	pin<14>	Connection to the 40 pin DIL plug to pin16 via level shifter
15	I/O_L01P_1	(F53) IC1 pin51	pin<15>	Connection to the 40 pin DIL plug to pin17 via level shifter
16	I/O_L01N_1	(F54) IC1 pin50	pin<16>	Connection to the 40 pin DIL plug to pin18 via level shifter
17	I/O_L02P_1	(F57) IC1 pin48	pin<17>	Connection to the 40 pin DIL plug to pin19 via level shifter
18	I/O_L02N_1	(F58) IC1 pin47	pin<18>	Connection to the 40 pin DIL plug to pin20 via level shifter
19	I/O_L03P_1 RHCLK0	(F60) IC1 pin45	pin<19>	Connection to the 40 pin DIL plug to pin21 via level shifter
20	I/O_L03N_1 RHCLK1	(F61) IC1 pin44	pin<20>	Connection to the 40 pin DIL plug to pin22 via level shifter
21	I/O_L06P_1 RHCLK6	(F67) IC1 pin39	pin<21>	Connection to the 40 pin DIL plug to pin27 via level shifter
22	I/O_L06N_1 RHCLK7	(F68) IC1 pin37	pin<22>	Connection to the 40 pin DIL plug to pin28 via level shifter
23	I/O_L07P_1	(F70) IC1 pin36	pin<23>	Connection to the 40 pin DIL plug to pin29 via level shifter
24	I/O_L07N_1	(F71) IC1 pin35	pin<24>	Connection to the 40 pin DIL plug to pin30 via level shifter
25	I/O_L03N_0	(F86)	pin<25>	Connection to the 40 pin DIL plug to pin31 via level shifter

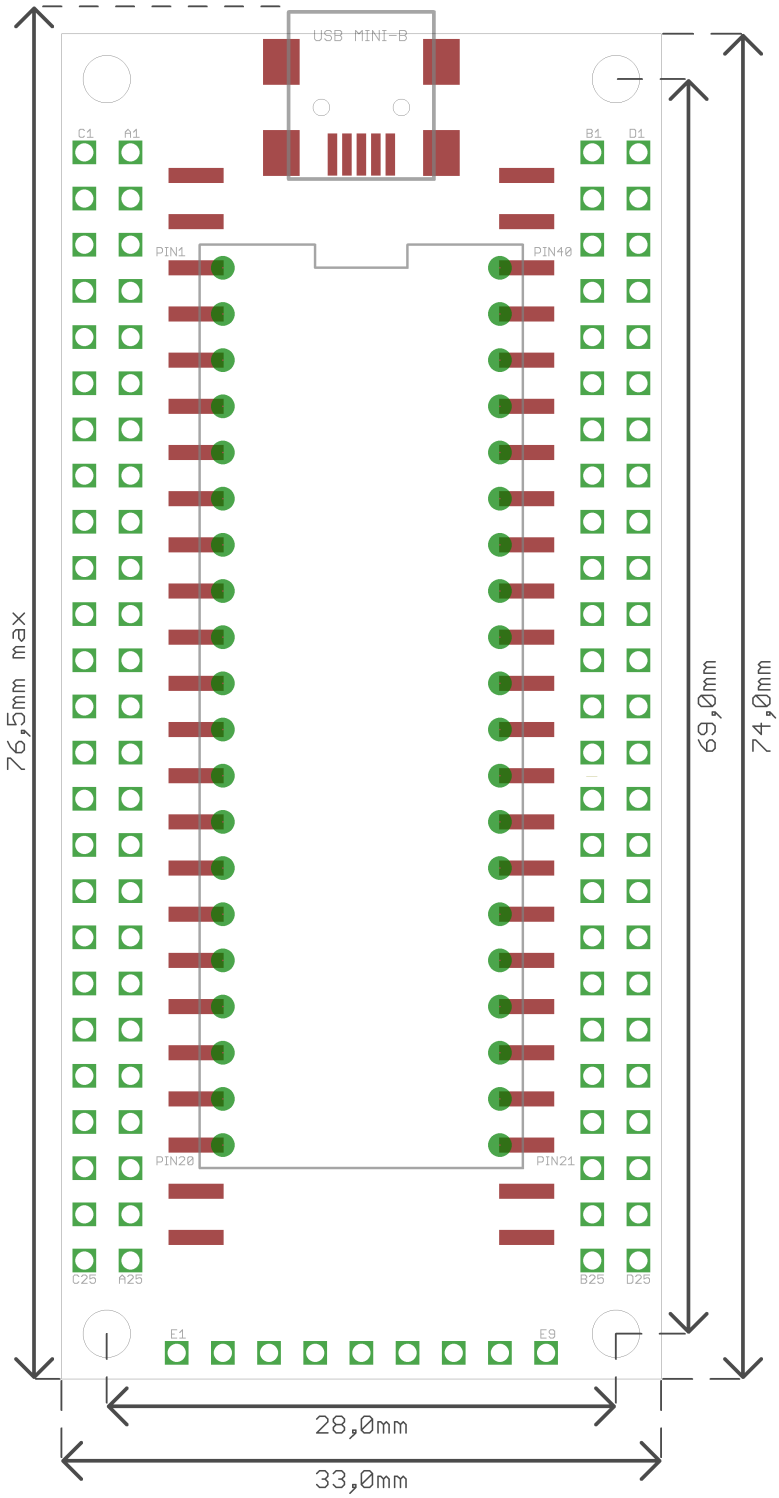
	GCLK7	IC1 pin34		
26	I/O_L02N_0 GCLK5	(F84) IC1 pin32	pin<26>	Connection to the 40 pin DIL plug to pin32 via level shifter
27	I/O_L02P_0 GCLK4	(F83) IC1 pin31	pin<27>	Connection to the 40 pin DIL plug to pin33 via level shifter
28	I/O_L01P_0	(F78) IC1 pin29	pin<28>	Connection to the 40 pin DIL plug to pin34 via level shifter
29	I/O_L01N_0	(F79) IC1 pin30	pin<29>	Connection to the 40 pin DIL plug to pin35 via level shifter
30	I/O_L03P_0 GCLK6	(F85) IC1 pin33	pin<30>	Connection to the 40 pin DIL plug to pin36 via level shifter
31	I/O	(F92) IC3 pin50	pin<31>	Connection to the 40 pin DIL plug to pin37 via level shifter
32	I/O_L07P_0 GCLK2	(F98) IC3 pin34	pin<32>	Connection to the 40 pin DIL plug to pin38 via level shifter
33	I/O_L01N_3	(F03) IC3 pin53	pin<33>	Connection to the 40 pin DIL plug to pin39 via level shifter
34	I/O_L01P_3	(F02) IC3 pin54	pin<34>	Connection to the 40 pin DIL plug to pin40 via level shifter
35	I/O_L02P_3	(F04) IC3 pin52	pin<35>	Connection to the 40 pin DIL plug to pin41 via level shifter
36	I/O_L02N_3 VREF3	(F05) IC3 pin51	pin<36>	Connection to the 40 pin DIL plug to pin42 via level shifter
37	I/O_L05P_0 GCLK10	(F90) IC3 pin48	pin<37>	Connection to the 40 pin DIL plug to pin43 via level shifter
38	I/O_L03P_3 LHCLK0	(F09) IC3 pin47	pin<38>	Connection to the 40 pin DIL plug to pin44 via level shifter
39	I/O_L03N_3 LHCLK1	(F10) IC3 pin46	pin<39>	Connection to the 40 pin DIL plug to pin45 via level shifter
40	I/O_L04P_3 LHCLK2	(F11) IC3 pin45	pin<40>	Connection to the 40 pin DIL plug to pin46 via level shifter

11. CON1 DIL Connector Layout and Dimensioning

GODIL48 module top view for 48 pin DIL mode:



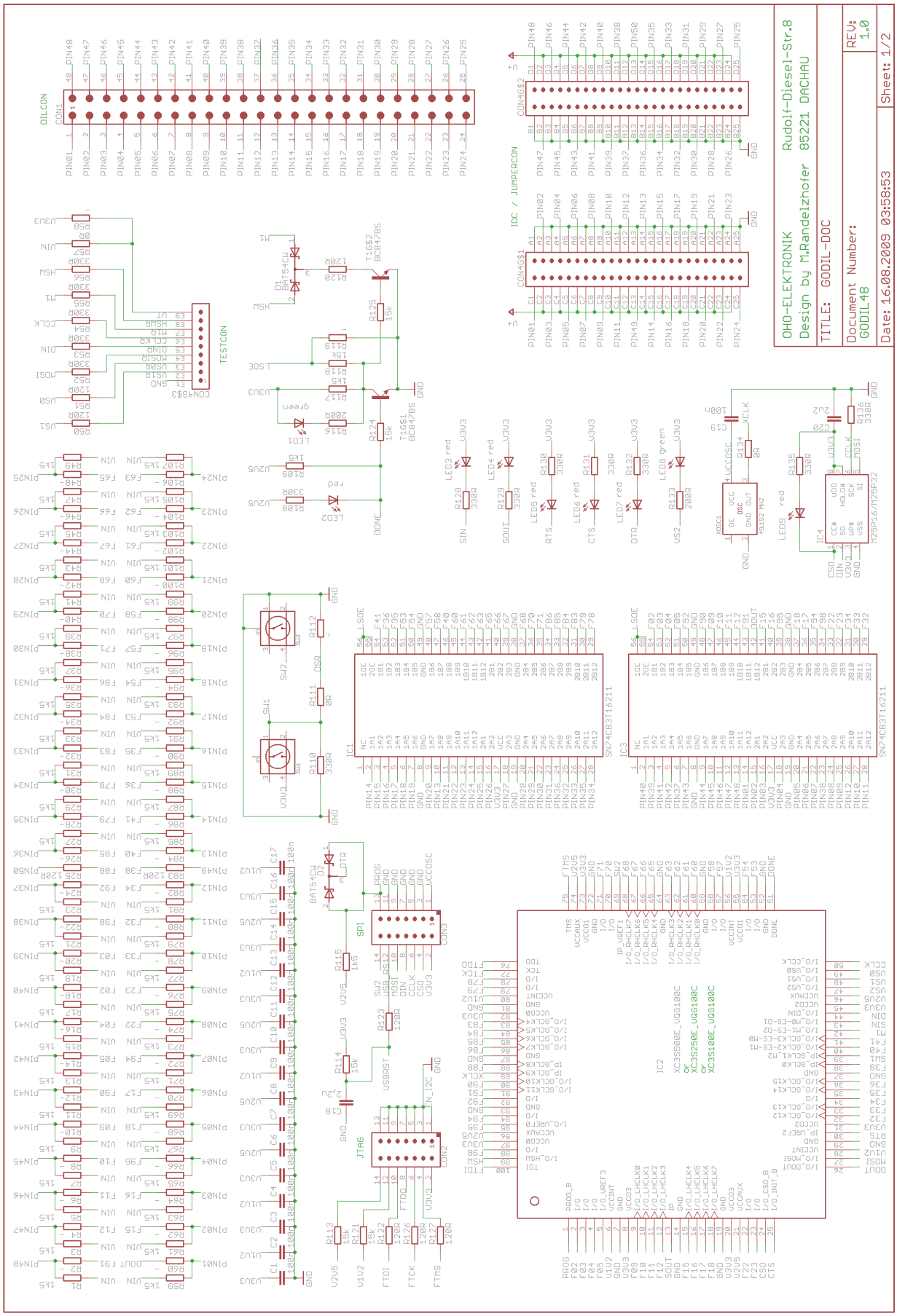
GODIL40 module top view for 40 pin DIL mode:



12. FPGA Design Support

VHDL and UCF design templates for 50, 48 and 40 pin configurations are available.

Schematics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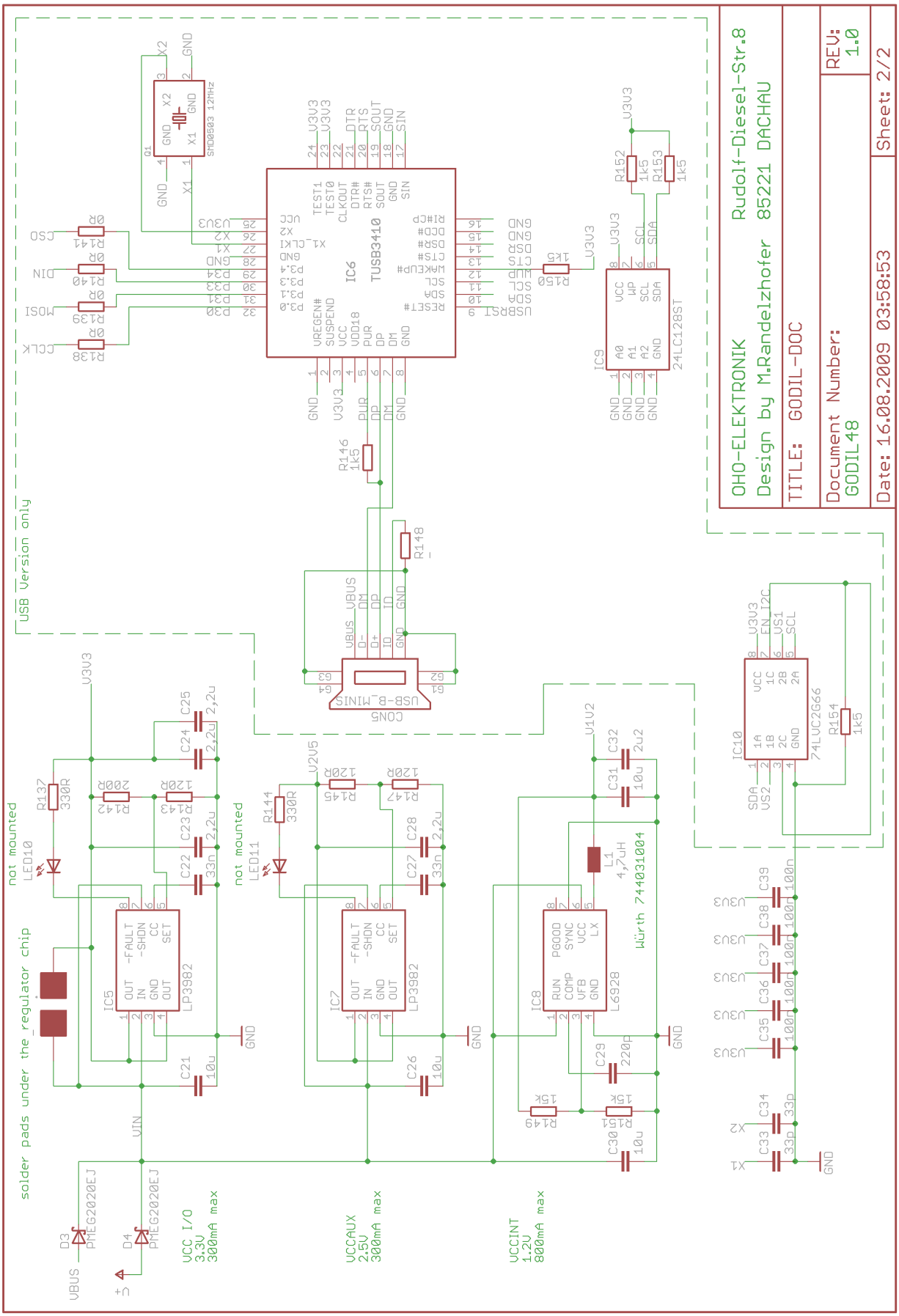
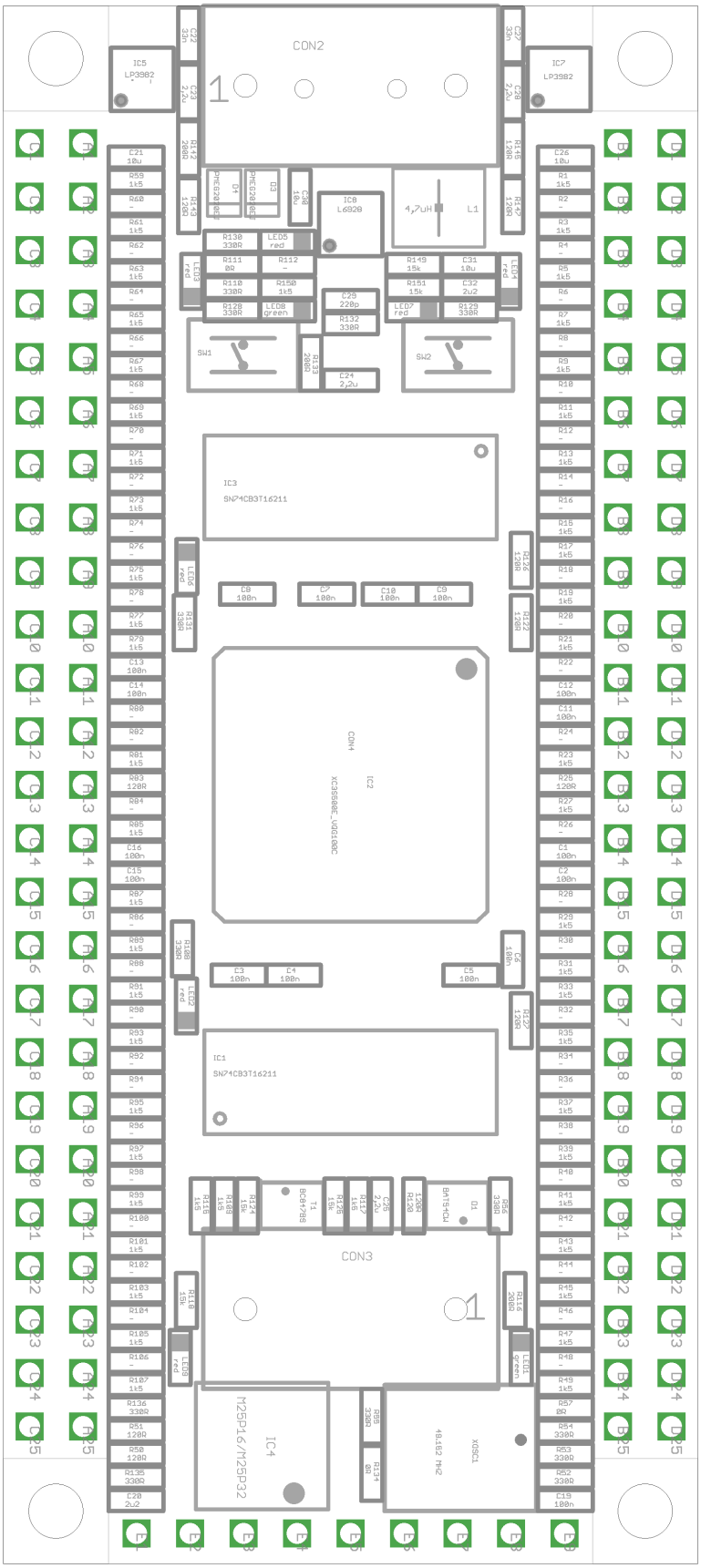
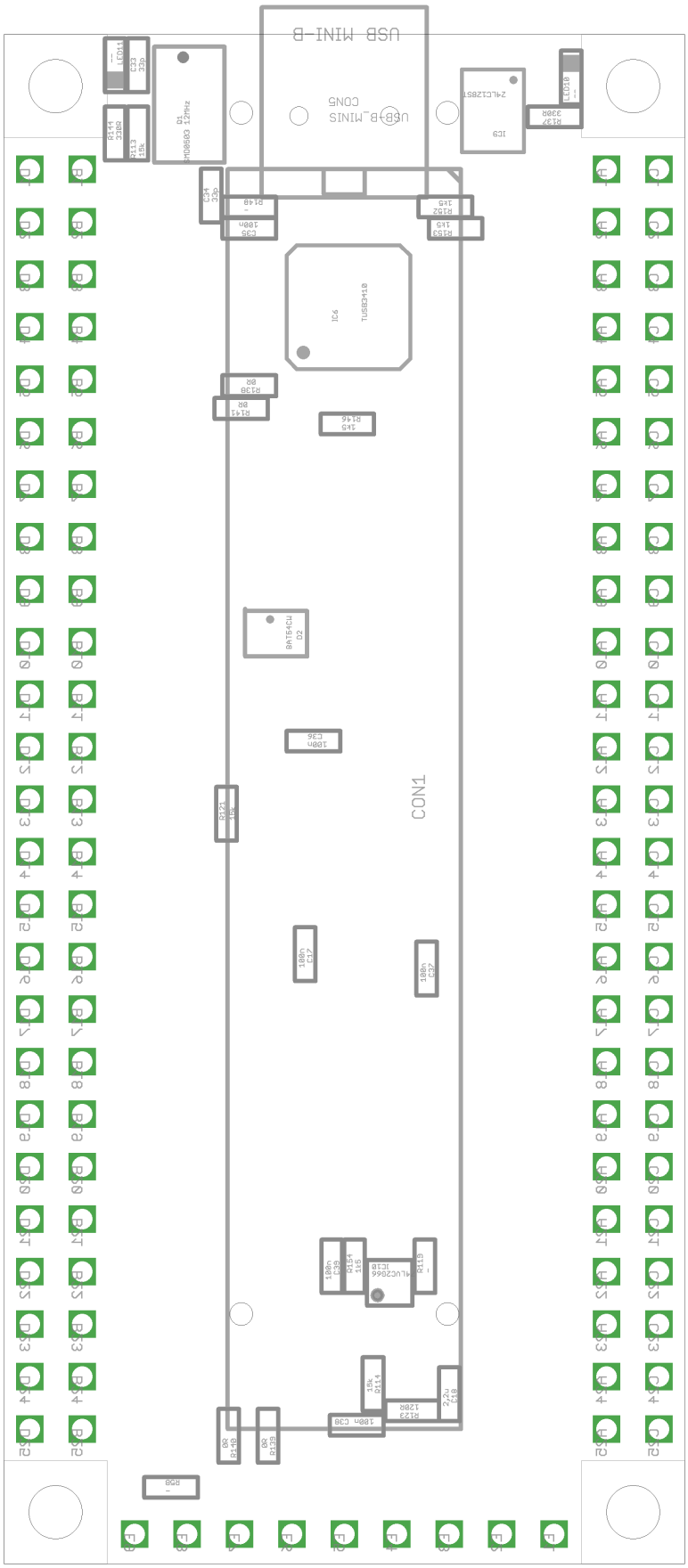
Rudolf-Diesel-Str.8
Design by M.Randelzhofer
85221 DACHAU
TITLE: GODIL-DOC
Document Number:
GODIL48
REV: 1.0
Date: 16.08.2009 03:58:53
Sheet: 1/2
DILCON
IDC / JUMPERCON
TESTCON
JTAG
SPI
XC3S50E_UQG100C
XC3S250E_UQG100C
or
XC3S100E_UQG100C
SN74CB3T16211
M25P16/M25P32


OHO-ELEKTRONIK
Rudolf-Diesel-Str.8
Design by M.Randelzhofer 85221 DACHAU
TITLE: GODIL-DOC
Document Number: GODIL48
REV: 1.0
Date: 16.08.2009 03:58:53
Sheet: 2/2
USB Version only
solder pads under the regulator chip
not mounted
not mounted
IC6 TUSB3410
IC5 LP3982
IC7 LP3982
IC8 L6928
Würth 744031004
74LVC2G66
24LC128ST
USB-B_MINIS
VCCIO 3.3V 300mA max
VCCAUX 2.5V 300mA max
VCCINT 1.2V 800mA max

13. Module Layout Top View



14. Module Layout Bottom View



15. Assembly variants

Different assembly options can be delivered.
GODIL modules can be assembled with the following Spartan-3E FPGAs:

- XC3S500E_VQG100C
- XC3S250E_VQG100C
- XC3S100E_VQG100C

The SPI Flash M25P32 is assembled for XC3S500E FPGAs.
The SPI Flash M25P16 is assembled for XC3S250E and XC3S100E FPGAs.

Different sizes like M25P40 (for faster erase time) can be custom assembled, level shifter can be omitted, and an industrial version of the whole module can be ordered (please talk to us).

For a future extension, an USB full speed interface option is planned.

Table of orderable GODIL standard options:

Ordering code	**Connector type**	**Comment**
GODIL_XC3S500E	plain board	500k S3E FPGA, without connectors
GODIL_XC3S250E		250k S3E FPGA, without connectors
GODIL40_XC3S500E	40 pin DIL mounted	500k S3E FPGA, bottom 40DIL connector, top headers
GODIL40_XC3S250E		250k S3E FPGA, bottom 40DIL connector, top headers
GODIL48_XC3S500E	48 pin DIL mounted	500k S3E FPGA, bottom 48DIL connector, top headers
GODIL48_XC3S250E		250k S3E FPGA, bottom 48DIL connector, top headers
GODIL50_XC3S500E	2 x 50 pin female headers mounted	500k S3E FPGA, 2x bottom female headers 50 pin
GODIL50_XC3S250E		250k S3E FPGA, 2x bottom female headers 50 pin

A XC3S100E FPGA can be ordered from 10 pieces.
A 3,3V version without level shifters can be ordered from 10 pieces.

16. Technical Specifications

FPGA:	Xilinx XC3S500E-4VQG100C Spartan-3E FPGA or Xilinx XC3S250E-4VQG100C Spartan-3E FPGA or Xilinx XC3S100E-4VQG100C Spartan-3E FPGA
Supply Voltage on any PIN:	3,5 - 5,5V
Size:	74 x 33mm 76 x 33mm incl. USB connector
Height PCB to Top:	max. 9mm
Height PCB to Bottom:	max. 12mm
Weight:	max. 30g

17. Literature

- [1] DS312 Xilinx Spartan-3E Complete Data Sheet
  http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf
- [2] DS097 Xilinx Parallel Cable IV
  http://www.xilinx.com/support/documentation/data_sheets/ds097.pdf
- [3] DS300 Xilinx Platform Cable USB
  http://www.xilinx.com/support/documentation/data_sheets/ds300.pdf
- [4] DS593 Xilinx Platform Cable USB-II
  http://www.xilinx.com/support/documentation/data_sheets/ds593.pdf
- [5] LP3982 National Semiconductor LDO CMOS Regulator
  http://www.national.com/ds/LP/LP3982.pdf
- [6] L6928 ST High Efficiency Monolithic Synchronious Step Down Regulator
  http://www.st.com/stonline/products/literature/ds/11051.pdf
- [7] TI SN74CB3T16211 24-Bit Fet Bus Switch
  http://focus.ti.com/lit/ds/symlink/sn74cb3t16211.pdf
- [8] TI USB Microcontroller
  http://www.ti.com/lit/gpn/tusb3410

18. USER MANUAL Revisions

Version	Date	Comments
V0.90	20/08/2009	Prerelease
V0.91	31/12/2009	Added dimensioning